ABSTRACT OF THE DISCLOSURE

A memory circuit includes a delay circuit for generating a delay clock signal by delaying a reference clock signal, a temperature detection circuit, and a voltage detection circuit. The temperature detection circuit detects the temperature of part around a memory and the voltage detection circuit detects the power-supply voltage of the memory. The delay circuit determines the delay amount of the delay clock signal according to at least one of temperature data detected by the temperature detection circuit and voltage data detected by the voltage detection circuit, whereby a circuit accessing the memory can supply a clock signal without being affected by the temperature change and/or the power-supply voltage fluctuation.